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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/429,446	10/28/1999	LYNDON W. GRAHAM	SEM4492P0771	5945

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EXAMINER
LEADER, WILLIAM T

ART UNIT	PAPER NUMBER
1742	

DATE MAILED: 06/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/429,446	GRAHAM ET AL.	
	Examiner	Art Unit	
	William T. Leader	1742	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 April 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *15-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *15-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 22 .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on April 4, 2003, has been entered.

2. On April 4, 2003, applicant filed a declaration under 37 CFR 1.131. Section 715.30 of the MPEP is directed the evaluation of 1.131 declaration in cases where the predictability of species in a genus is in question, and states that where generic claims have been rejected on a reference which discloses a species not antedated by the affidavit or declaration, the rejection will *not* ordinarily be withdrawn unless the applicant is able to establish that he or she was in possession of the generic invention prior to the effective date of the reference. In the present application, references applied in the previous office action disclose a plurality of noble metal species. Lyndon Graham's notebook, attached to the declaration as exhibit A, demonstrates that work was performed using an electroplating solution containing platinum. Platinum is one species in the genus of noble metals. The declaration does not point to work with any other noble metal. Thus, applicant has

demonstrated only the completion of the invention with respect to platinum. Applicant points out that platinum is a noble metal, and apparently considers this single species to be representative of the genus. In order to be effective in overcoming the rejection, the behavior of the species in the genus of noble metals must be predictable. In evaluating the declaration, the Examiner adopts the position that in the context of the claimed invention, the behavior of noble metals is predictable, and that the behavior of any one species in the genus of noble metals is indicative of the behavior of any other metal in the genus. Consequently, the declaration filed on April 4, 2003, under 37 CFR 1.131 is sufficient to overcome the Jorne et al, Reid et al, Shue et al Ting et al, Erb and Taylor et al references applied in the previous office action.

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

Claim Rejections - 35 USC § 103

4. Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970).

5. The Poris et al patent (US 5,256,274) is directed to a process for electrolytically depositing a metal onto a semiconductor wafer (abstract). The metal may be copper or the noble metals silver or gold (column 3, line 3). Using copper as an example, Poris et al explain that deposition of metal occurs by the electrolysis of a copper ion-containing aqueous electrolyte. The physical laws governing this reaction were explained by Faraday in 1833. By passing an electric charge through the two electrodes immersed in the electrolyte, metal is stripped from the anode and deposited on the cathode. Positive copper ions are attracted to the negative cathode where they combine with electrons yielding neutral copper which is plated onto the electrode (column 4, lines 1-20).

6. As shown in figure 2 of Poris, a dielectric layer is formed on the silicon wafer. Then, a thin diffusion barrier layer is deposited. This layer serves the functions of providing an electrically conducting layer to allow uniform metal electrodeposition across the entire wafer surface and preventing interaction of the electrodeposited metal with the silicon or dielectric oxide (column 6, lines 38-44 and column 11, lines 53-57). Next, a nucleation layer is deposited. This layer provides excellent ohmic contact to the diffusion barrier and provides an excellent nucleating surface for the electrodeposited metal. It may be platinum or other noble metal (column 6, line 65 to column 7, line 11). This is the layer on which electrodeposition takes place, and it corresponds to applicant's seed layer. Only several monolayers are required for

good nucleation properties and a thickness of 250 angstroms has been successfully used (column 7, lines 12-14). This thickness falls within the range of no more than 1000 angstroms recited in instant claim 15. A patterned mask is formed, and metal is electroplated onto the workpiece. Figure 2 shows the openings in the dielectric layer E into which metal is plated. A size reference line indicating the length of 1 μM (micron) is shown in figure 2. Comparison of the openings with the size reference line shows that the openings are submicron in size, as recited in instant claim 15.

7. Claim 15 differs from the process of Poris by reciting that electroplating power is applied at a low current for a first period of time and at a higher current for a second period of time. The Lowenheim text, *Electroplating*, includes a chapter directed to Plating on Nonconductors. Lowenheim states that "To electroplate on a nonconducting medium, it is necessary that the surface of that medium be made conductive in some way" (page 417). One method disclosed by Lowenheim it to form an electrically conductive seed layer by electroless deposition. Once a nonconducting surface such as a plastic has been rendered catalytic, it is ready for the deposition of electroless copper or nickel, to be followed by conventional electroplating. Lowenheim notes that since only the surface of the nonconductive plastic workpiece where the electroless layer has been formed is conductive, and the electroless deposit is quite thin, the conductivity of the part is not comparable to

that of metallic articles where the entire thickness of the article is conductive. Lowenheim states "electroplating must be started at relatively low current densities to avoid burning at contact points" (page 423).

8. Lowenheim teaches that electrochemical processes such as electroplating follow Faraday's Laws which may be stated as follows:

1. The amount of chemical change produced by an electric current is proportional to the quantity of electricity that passes, and

2. The amounts of different substances liberated by a given quantity of electricity are proportional to their chemical equivalent weights.

These laws may be expressed in the form of the equation:

$$g = Iet \,/\, 96{,}500$$

where g = grams of substance reacting, I = current in amperes, e = chemical equivalent weight, and t = time in seconds. For an electrodeposition process, the grams of substance reacting is the amount metal deposited at the cathode. This equation indicates that there is an inverse relationship between the current applied in an electrodeposition process and the time it takes to deposit a given amount of metal. Lower current leads to longer deposition time, while higher current results in shorter deposition times. This fundamental relationship of electrodeposition provides motivation for using higher current because it allows the process to be

completed more quickly, resulting in more efficient and economical operation. See pages 12-13.

9. The Ameen et al patent is cited to illustrate an application of the procedure taught by Lowenheim, and to provide additional motivation for initiating electroplating on a seed layer at a low current density followed by higher current densities. The patent is directed to a method for metallizing polymeric films by electrodeposition. The metallized films may be used in the production of circuit boards (column 1, lines 31-36). Ameen et al teach that when the non-metallic, electrically insulating substrate is a flexible polymeric sheet, the metal, such as copper, may be electrodeposited directly on a flash of metal which has been sputtered, vapor deposited, electrolessly deposited, or adhered by similar techniques on the sheet (column 1, lines 37-41). Thus, Ameen teaches the preliminary deposition of a current-carrying metallic seed layer. Conventional electrodeposition methods for copper on polymeric sheets use current densities which result in lengthy deposition times (column 2, lines 22-26). Like Lowenheim, Ameen et al recognize that the rate of metal deposition is basically dependent on the current which can be applied to the metal on the substrate, and that the current is limited by the thickness as well as the current-carrying characteristics of the metal on the substrate (column 2, lines 34-40). Ameen et al teach that the problem of long deposition time can be overcome by a method in which the current applied to the

substrate is increased as the deposition process is carried out. In the invention of Ameen et al, the anode electrodes opposed to the cathodic polymeric sheet to be plated are energized in groups. As metal is deposited onto the initial flash of metal on the substrate by the initial groups of anodes, the increased current carrying capacity of the thicker metal is utilized to allow subsequent groups of anodes to have higher energization levels. The ever increasing thickness of the metal on the substrate, and its increasing current-carrying capacity, is used to increase the electrodeposition rate of metal by continually increasing the current based on the current carrying capacity of the deposited metal (column 10, lines 39 – column 11, line 3). More specifically, the first group of anodes is energized at a level which the flash metal seed layer on the substrate can handle. The first group of anodes deposits metal from the electrolytic solution onto the flash metal, thereby building up the thickness of the metal on the substrate. Eventually, each group of anodes can be energized at its desired operating level (column 11, lines 4-42).

10. The prior art of record is indicative of the level of skill of one of ordinary skill in the art. It would have been obvious at the time the invention was made to have begun the electrodeposition step of Poris at a low current density and to have increased the current density after a period of time in which the thickness and current-carrying capacity of the plated layer had grown as taught by Lowenheim and Ameen et al because burning of the initially deposited seed layer would have

been avoided by using the lower current density, and the rate of deposition would have been increased by using higher current densities, thereby shortening the time needed to deposit the desired thickness of metal and performing the deposition process more efficiently.

11. Claims 16-19 and 32-34 rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970) as applied to claim 15 above, and further in view of Young et al (4,705,606) and Tamaki et al (5,227,001).

12. Claims 16, 17 and 19 relate to a step of prerinsing, while claims 32-34 relate to a step of precleaning. The Young et al patent is directed to a process for depositing metallic interconnections for integrated circuits on a semiconductor wafer and discloses the use of a standard cleaning procedure for silicon wafers prior to subsequent processing. The cleaning procedure includes treatment in an acidic solution as recited in instant claims 17 and 34, and rinsing in deionized water recited in instant claims 19 and 33. The wafer is spun dried as recited in instant claim 19. See column 3, lines 25-46. The Tamaki et al patent is directed to semiconductor wafer processing and discloses a step of cleaning. The wafer is subjected to cleaning with water mist sprayed by nozzles. The nozzles may transmit ultrasonic vibrations to the mist, resulting in a forceful cleaning of the

wafer. During cleaning, the wafer may be rotated at a relatively low speed. The wafer is then subjected to spin drying at a higher speed. See column 8, lines 35-62. It would have been obvious at the time the invention was made to have precleaned and prerinsed a semiconductor wafer prior to plating in the process of Poris because contaminants would have been removed as taught by Young et al and Tamaki et al. While Young et al and Tamaki et al disclose the use of spinning to remove liquid from the wafer being treated, spinning to remove plating solution as recited in instant claim 18 is not specifically mentioned. However, since the references show that spinning is effective to remove liquid, one of ordinary skill in the art would have recognized that spinning would have been effective in removing excess plating solution.

13. Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970) as applied to claim 15 above, and further in view of Inoue et al (5,556,814).

14. Claim 20 further differs from the process of Poris by reciting that the electroplating solution includes platinum. As indicated above, Poris discloses that semiconductors can be metallized with copper, or either of the noble metals gold or silver. The Inoue et al patent is directed to forming wiring for integrated circuits on

a semiconductor wafer by electroplating. The electroplated metal may be copper, gold, platinum or palladium (column 6, lines 34-38). It would have been obvious to have utilized an electroplating solution containing platinum in place of the copper or gold taught by Poris because platinum is a recognized alternative to copper and gold for metallizing a semiconductor as shown by Inoue et al.

15. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970) and further in view of Inoue et al (5,556,814) as applied to claim 20 above, and additionally in view of Abys (4,427,502) and Dubin et al (5,972,192).

16. Claims 21-26 relate to process parameters used in the electrodeposition. The Abys patent is directed to a process for electroplating platinum and platinum alloys. The platinum concentration ranges from 0.005 molar to saturation (column 4, lines 40-41). This range includes the range recited in instant claim 21. The pH is preferably within the range of 10 to 12.5 (column 3, lines 53-57). This range includes the range of 11-12 recited in claim 24. Abys discloses that a preferred temperature range is 50 to 70°C. This range falls within the range of 40-80°C recited in claim 22. Abys discloses the use of a broad current range (column 4, lines 43-45) but does not specify that pulsed current should be used. Dubin et al disclose that pulse current as recited in instant claim 25 may advantageously be used in

electroplating into the surface features of a semiconductor wafer. See the abstract. Poris also recognizes that pulse plating may be used (column 8, lines 45-47). It would have been obvious at the time the invention was made to have utilized a platinum plating bath and plating parameters as disclosed by Abys to metallize a semiconductor wafer in the process of Poris et al because these parameters are effective in depositing platinum, and to have used pulsed current as disclosed by Poris and Dubin et al because it is effective in filling surface features of a semiconductor wafer. Current density is a result-effective parameter, the optimization of which falls within the skill of the ordinary worker in the art.

17. It is noted that in one embodiment of Poris, electrodeposition was carried out at a DC cathode current density of 5 mA/cm^2 (column 12, line 24). In choosing the anode current density, Poris notes that reference was made to printed circuit board literature (column 8, lines 59-62). Thus, there is a recognition by Poris that prior art (such as the Ameen et al patent) relating to the production of printed circuit boards is relevant to processes of metallizing semiconductor wafers.

18. Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poris (5,256,274) in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970) and further in view of Inoue et al (5,556,814) as applied to claim 20 as

applied to claim 20 above, and further in view of additional pages of Lowenheim and Dubin (5,972,192).

19. Claims 27-31 relate to process parameters used in the deposition of platinum. Lowenheim discloses a number of different electroplating baths for the deposition of platinum (page 300). Bath "S" has a pH of 2 which falls within the range recited in instant claim 27. The platinum concentration of this bath is 5 g/l which falls within the range recited in instant claim 28. Lowenheim does not specify the use of pulsed current. As discussed above, Poris and Dubin et al disclose that pulse current as recited in instant claim 29 may advantageously be used in electroplating into the surface features of a semiconductor wafer. It would have been obvious at the time the invention was made to have utilized a platinum plating bath and plating parameters as disclosed by Lowenheim to metallize a semiconductor wafer in the process of Poris because these parameters are effective in depositing platinum, and to have used pulsed current as disclosed by Poris and Dubin et al because it is effective in filling surface features of a semiconductor wafer. Current density is a result-effective parameter, the optimization of which falls within the skill of the ordinary worker in the art.

20. Claims 15 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al (5,789,320) in view of either Nitayama et al (6,236,079) or Lu

et al (5,595,928) and further in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970).

21. The Andricacos et al patent is directed to a process for making small geometry gigabit scale dynamic random access memory (DRAM) microelectronic devices. The process includes the step of electroplating a noble metal to form electrodes (column 1, line 66 to column 2, line 1). A plating base (seed layer), which typically has a thickness of 300-2000 angstroms, but may be as thin as 30 angstroms, is first formed (column 2, lines 49-52). One of the procedures used to deposit the electrodes is a damascene process shown in figures 3f-3l. A masking layer is deposited on the substrate and patterned to form the features into which the electrode material is to be deposited, a seed layer is blanket coated onto the masking layer, the structure is blanket electroplated with the noble metal, and planarization is conducted by chemical mechanical polishing (column 5, line 61 to column 6, line 1). The noble metal deposited may be platinum (column 6, lines 59-62).

22. Claim 15 differs from the process of Andricacos et al by reciting that the features into which the noble metal is electroplated are submicron features, and reciting that electroplating power is applied at a low current for a first period of time and at a higher current for a second period of time. As noted above, Andricacos states that the process is for producing high density DRAM storage

elements, and specifically refers to gigabit scale DRAM (column 1, line 16; column 1, line 67 to column 2, line 1). Andricacos is silent as to the typical dimensions utilized in gigabit scale DRAM devices.

23. The Nitayama et al patent is directed to DRAM devices. Nitayama et al teach that a 0.25 micron design rule is usable in a 256 Mbit DRAM (column 1, lines 10-13), while 1 Gbit DRAM devices follow a 0.18 micron design rule (column 11, lines 45-46). The Lu et al patent is directed to high density DRAM devices and discloses that the storage capacitors are usually built on P-doped single crystal silicon substrates using n-channel field effect transistors (FETs) as the pass transistor, as is currently used in the manufacture of DRAMs (column 4, lines 7-10). The FET gate electrode is expected to be less than a quarter micrometer in size (column 6, lines 36-39). Thus, as shown by Nitayama et al and Lu et al the dimensions utilized by Andricacos in making a high density gigabit scale DRAM devices are submicron dimensions as recited by applicant.

24. As indicated above, Andricacos discloses the use of extremely thin seed layers, some having a thickness of only 300 angstroms or less. Such a thin layer has a low electrical conductivity and is subject to burning. The Lowenheim text and Ameen patent are taken as above and show that in processes for electrodeposition over a seed layer it is known to begin plating at a low current density and to subsequently increase the current density.

25. It would have been obvious at the time the invention was made to have begun the electrodeposition step of Andricacos at a low current density and to have increased the current density after a period of time in which the thickness and current-carrying capacity of the plated layer had grown as taught by Lowenheim and Ameen et al because burning of the initially deposited seed layer would have been avoided by using the lower current density, and the rate of deposition would have been increased by using higher current densities, thereby shortening the time needed to deposit the desired thickness of noble metal and performing the deposition process more efficiently. If not inherent in Andricacos, it would also have been obvious to have utilized submicron features in the DRAM of Andricacos since features of this size are conventional in the fabrication of the high density 1 gigabit DRAMs discussed by Andricacos as shown by Nitayama et al and Lu et al.

26. Claims 16-19 and 32-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al (5,789,320) in view of either Nitayama et al (6,236,079) or Lu et al (5,595,928) and further in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970) as applied to claims 15 and 20 above, and additionally in view of Young et al (4,705,606) and Tamaki et al (5,227,001).

27. As discussed above, claims 16, 17 and 19 relate to a step of prerinsing, while claims 32-34 relate to a step of precleaning. The Young et al patent and Tamaki et

al patent are taken as above. It would have been obvious at the time the invention was made to have precleaned and prerinsed a semiconductor prior to plating in the process of Andricacos et al because contaminants would have been removed as taught by Young et al and Tamaki et al. While Young et al and Tamaki et al disclose the use of spinning to remove liquid from the wafer being treated, spinning to remove plating solution as recited in instant claim 18 is not specifically mentioned. However, since the references show that spinning is effective to remove liquid, one of ordinary skill in the art would have recognized that spinning would have been effective in removing excess plating solution.

28. Claims 21-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al (5,789,320) in view of either Nitayama et al (6,236,079) or Lu et al (5,595,928) and further in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970) as applied to claims 15 and 20 above, and further in view of Abys (4,427,502) and Dubin et al (5,972,192).

29. As previously observed, claims 21-26 relate to process parameters used in the electrodeposition of platinum. The Abys and Dubin et al patents are taken as above. It would have been obvious at the time the invention was made to have utilized a platinum plating bath and plating parameters as disclosed by Abys to metallize a semiconductor wafer in the process of Andricacos et al because these

parameters are effective in depositing platinum, and to have used pulsed current as disclosed by Dubin et al because it is effective in filling surface features of a semiconductor wafer. Current density is a result-effective parameter, the optimization of which falls within the skill of the ordinary worker in the art.

30. Claims 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Andricacos et al (5,789,320) in view of either Nitayama et al (6,236,079) or Lu et al (5,595,928) and further in view of the Lowenheim text *Electroplating* and Ameen et al (US 5,685,970) as applied to claims 15 and 20 above, and further in view of additional pages of Lowenheim and Dubin et al (5,972,192).

31. Claims 27-31 relate to process parameters used in the deposition of platinum. Lowenheim and Dubin et al are taken as above. It would have been obvious at the time the invention was made to have utilized a platinum plating bath and plating parameters as disclosed by Lowenheim to metallize a semiconductor wafer in the process of Andricacos et al because these parameters are effective in depositing platinum, and to have used pulsed current as disclosed by Dubin et al because it is effective in filling surface features of a semiconductor wafer. Current density is a result-effective parameter, the optimization of which falls within the skill of the ordinary worker in the art.

32. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The Borrione et al patent (US 5,207,883) is directed to an electrolyzer for use in an electrolysis process. At column 4, lines 3-10, Borrione et al give the formula for electrical resistance. This formula is

$$R = pL / A$$

where R is the resistance in micro-ohms, p is the resistivity in micro-ohms/centimeter, L is the length in centimeters, and A is the cross sectional area in square centimeters. This formula shows that as the cross sectional area of a conductor decreases, the resistance to current flow of the conductor increases. Thus, the resistance of a thin seed layer, which would have a small cross section, would be high. As metal was deposited onto the seed layer and the cross section increased, the resistance would become lower.

33. The Nakakoji et al patent (US 5,403,468) is directed to electroplating tin on a steel strip. As column 5, lines 36-38, Nakakoji et al indicate that the electroplating current passing through the workpiece causes resistance heating to occur. The degree of heating would depend on the amount of current and the resistance of the workpiece. As shown by formula above, the resistance is proportional to cross sectional area. Thus, an article with a smaller cross section would exhibit a greater degree of resistance heating.

34. The Goldberg patent (US 5,484,518) was cited in the Information Statement filed on January 22, 2002 and is directed to an electroplating process useful in the fabrication of printed circuit boards. Goldberg includes the observation at column 8, lines 16-20, that "Theoretically, a low initial current density should be preferred with current density increased as an initial deposit is formed. This would be expected to prevent burnoff of the thin conversion coating." This recognition of accepted plating theory is the same as that taught by Lowenheim, i.e. that a low initial current density should be used in plating on a nonconductor to avoid burning the thin seed layer, and that after a period of time in which an initial deposit is formed, the current should be increased.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to William T. Leader whose telephone number is 703-308-2530. The examiner can normally be reached on Mondays-Thursdays and alternate Fridays, 7:30-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King, can be reached on 703-308-1146. The fax phone numbers for the organization where this application or proceeding is assigned are

703-872-9310 for regular communications and 703-872-9311 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0661.

William Leader
June 10, 2003

ROY KING
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 1700